Feasibility of T/R Module Functionality in a Single SiGe IC

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GEDC

Georgia Institute of Technology

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
01 MAY 2007	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Feasibility of T/R Module Functionality in a Single SiGe ICFeasibility ICDr	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Georgia Institute of Technology**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM202171., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

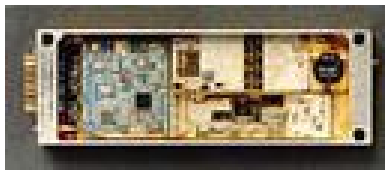
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**24**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

SiGe Single-Chip T/R Program

1990's

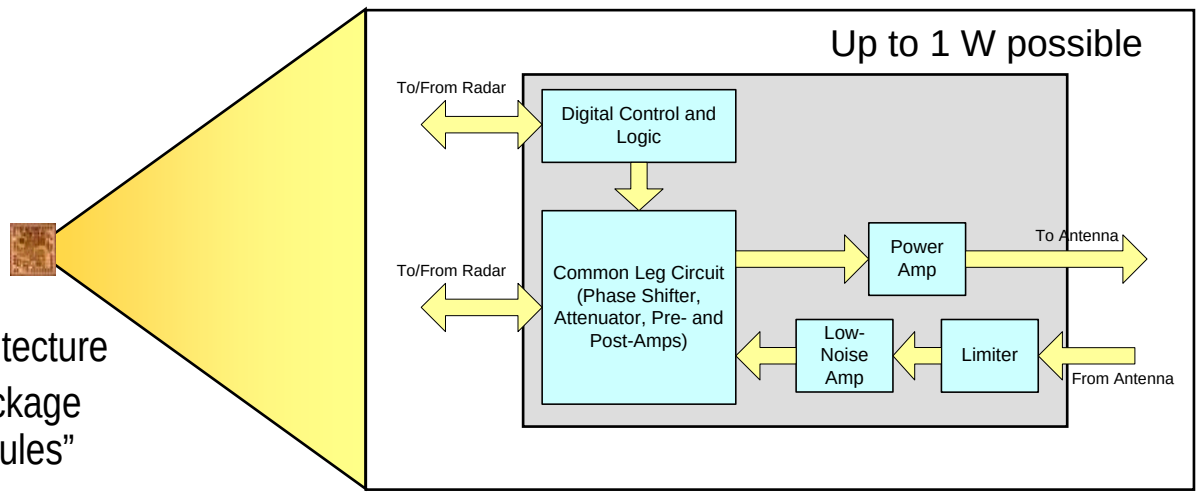
- Multi-chip module
- Expensive (~ $1000)
- High power
- Cost drivers:
  - MMIC area
  - Touch labor
  - Packaging



- GTRI and GEDC co-development
- Full Transmit/Receive module functionality in a single chip
- Currently developing devices
- Integrated chips to be available in FY07

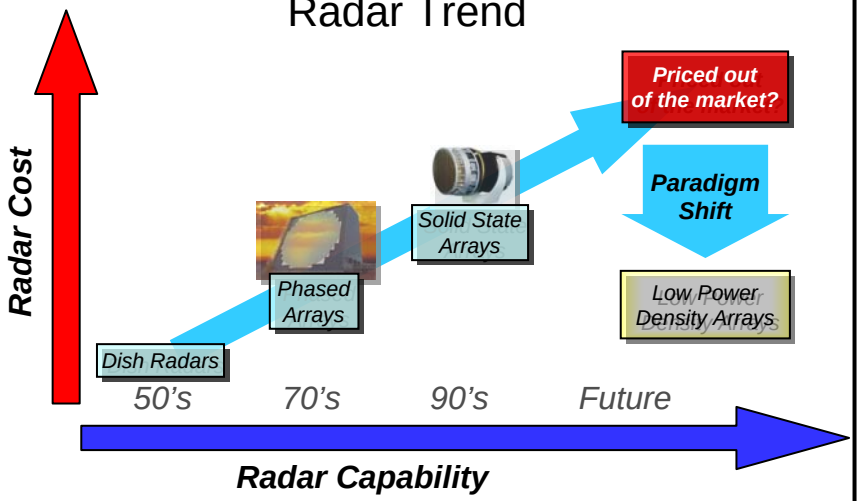
Future

- Single chip "module"
- Cheap (< $10)
- Low power
- New cost paradigm:
  - Multi-chip panel architecture
  - Spread labor and package cost over many "modules"



Redefining Future Radar Technology

Radar Trend



Low Power Density (LPD) Paradigm Shift

1990's

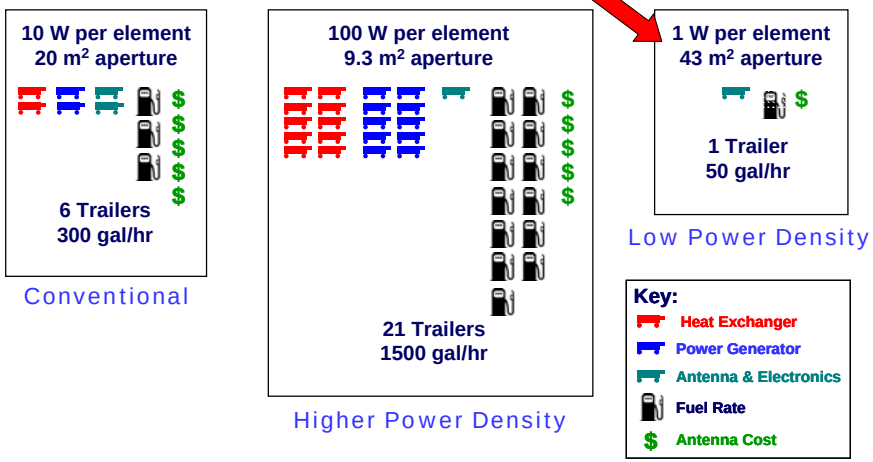
- Multi-chip module
- Expensive (~ $1000)
- High power
- Cost drivers:
  - MMIC area
  - Touch labor
  - Packaging

Future

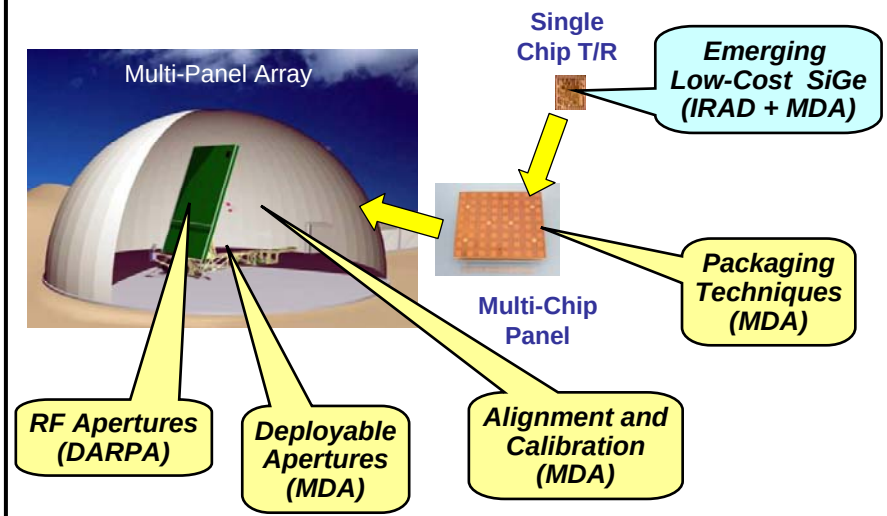
- Single chip "module"
- Cheap (< $10)
- Low power
- New cost paradigm:
  - Multi-module panel architecture
  - Spread labor and package cost over many "modules"

Low Power Density Benefits

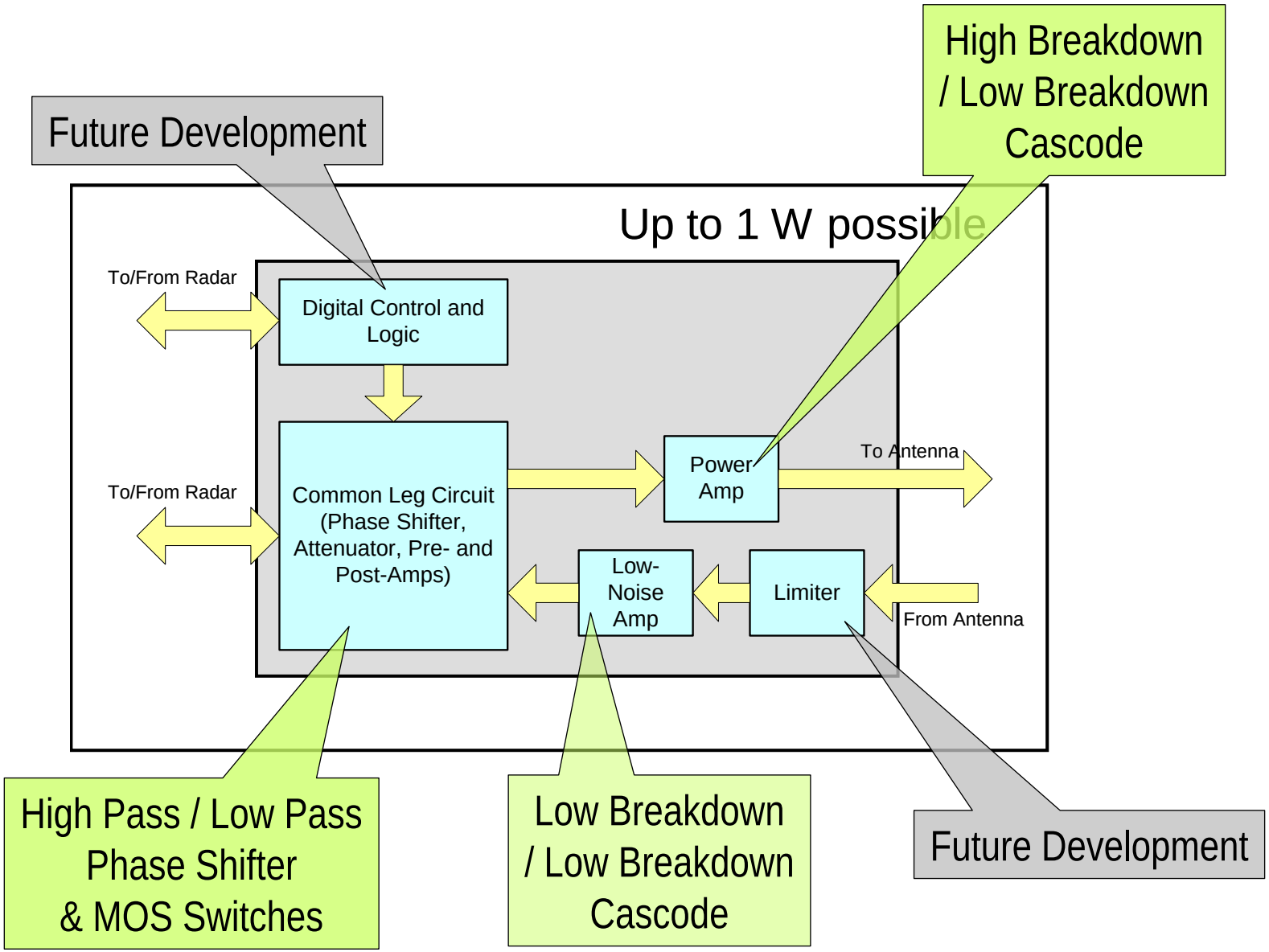
Large LPD antennas reduce cost and system footprint



Georgia Tech Research

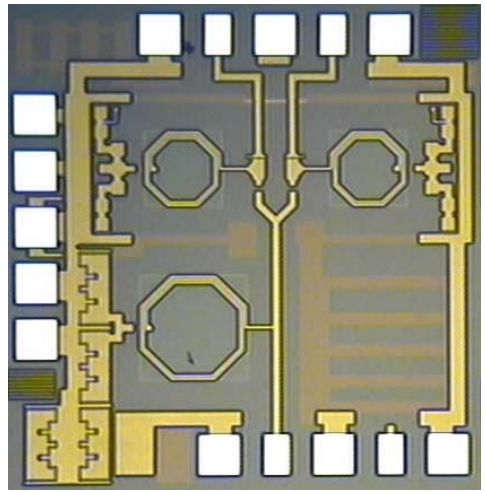


SiGe T/R Chip Development



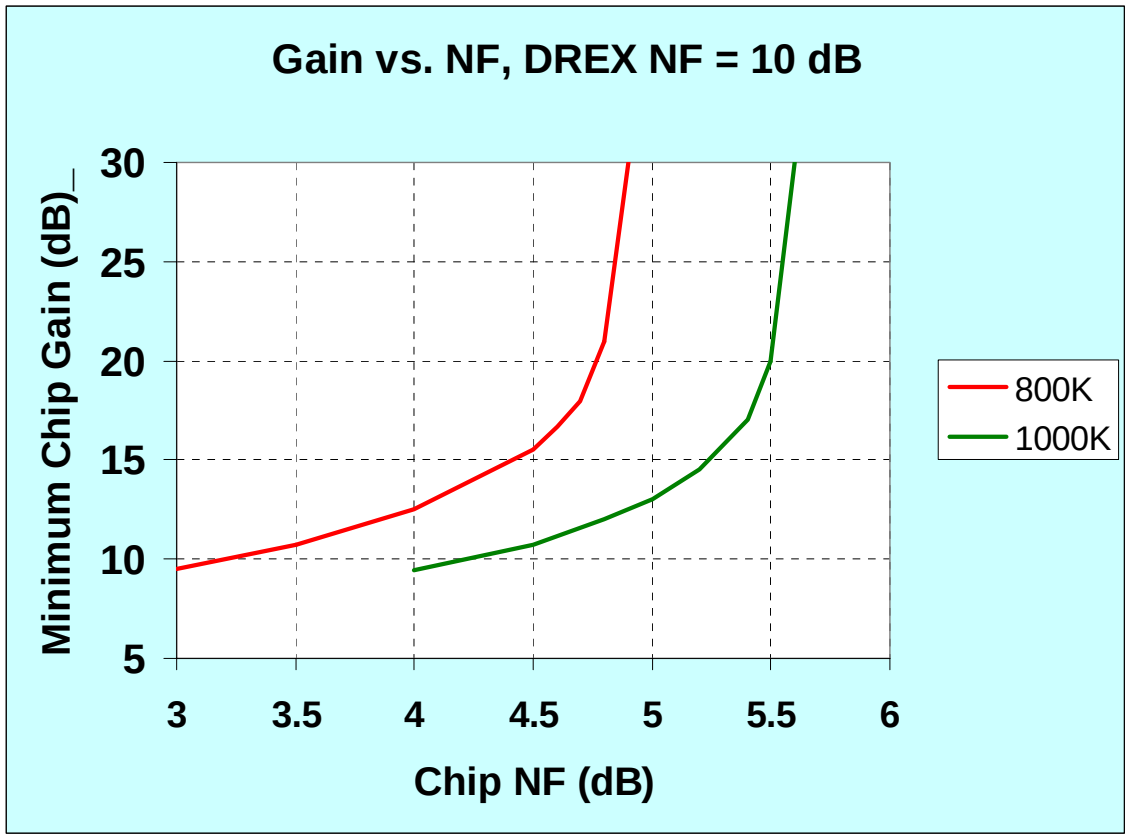
Accomplishments to Date

- ✓ Developed detailed T/R chip requirements
- ✓ Developed preliminary design
- ✓ Reviewed and Analyzed preliminary design
- ✓ Trade off design, specifications, and performance
- ✓ Designed and fabricated critical components
- ✓ Tested components



Gain / Noise Figure Requirements

- Requirements based on:
  - Overall system noise temperature of 800K (Objective) 1000K (Threshold)
  - Assumed Digital Receiver/Exciter (DREX) input NF = 10 dB



Phase Shifter Bit Requirements

At least 4 bits required for negligible gain loss

Number of Bits, N	Gain Loss (dB)
2	-1.000
3	-0.229
4	-0.056
5	-0.014
6	-0.003

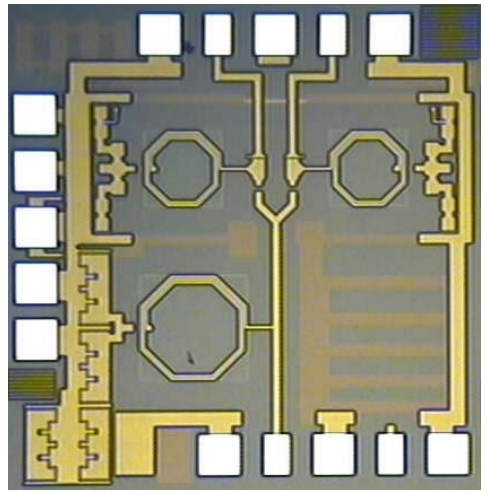
Increase to 5 bits preferable for low sidelobe performance

Number of bits	Minimum bit size (degrees)	RMS Phase Error (degrees)
2	90	26.0
3	45	13.0
4	22.5	6.5
5	11.25	3.2
6	5.625	1.6
7	2.8125	0.8

4-bit threshold and 5-bit objective requirements selected

Component Results to Date

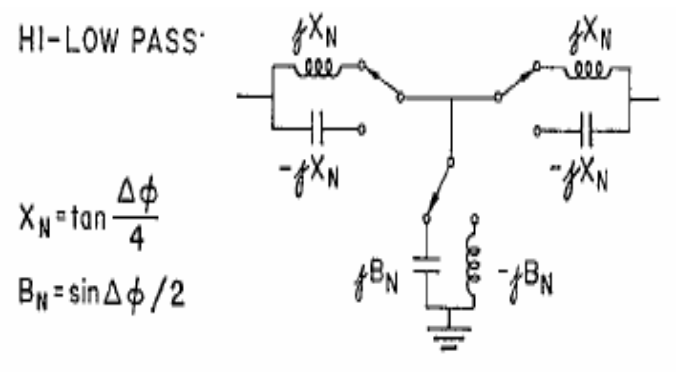
- ✓ Hi Pass / Lo Pass Phase Shifter
- ✓ MOS Switches
- ✓ Cascode LNA
- ✓ Cascode Pre Amp
- ✓ Cascode Power Amp



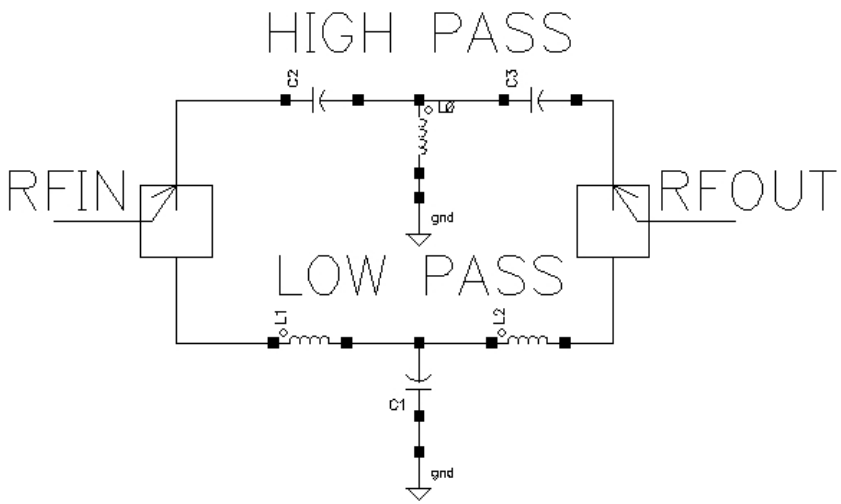
Hi-Low Pass Shifter

- **Hi-Low pass phase shifter provides flat phase response**
- **Shift is relative phase between low pass and high pass**
- **Very broadband and easier to control than reflection shifter**
- **Higher values of shift require more elements**
- **Switch and filter sections can be designed independently**
  (if filter and switch S11 < -20 dB)

Hi-Low Pass Schematic

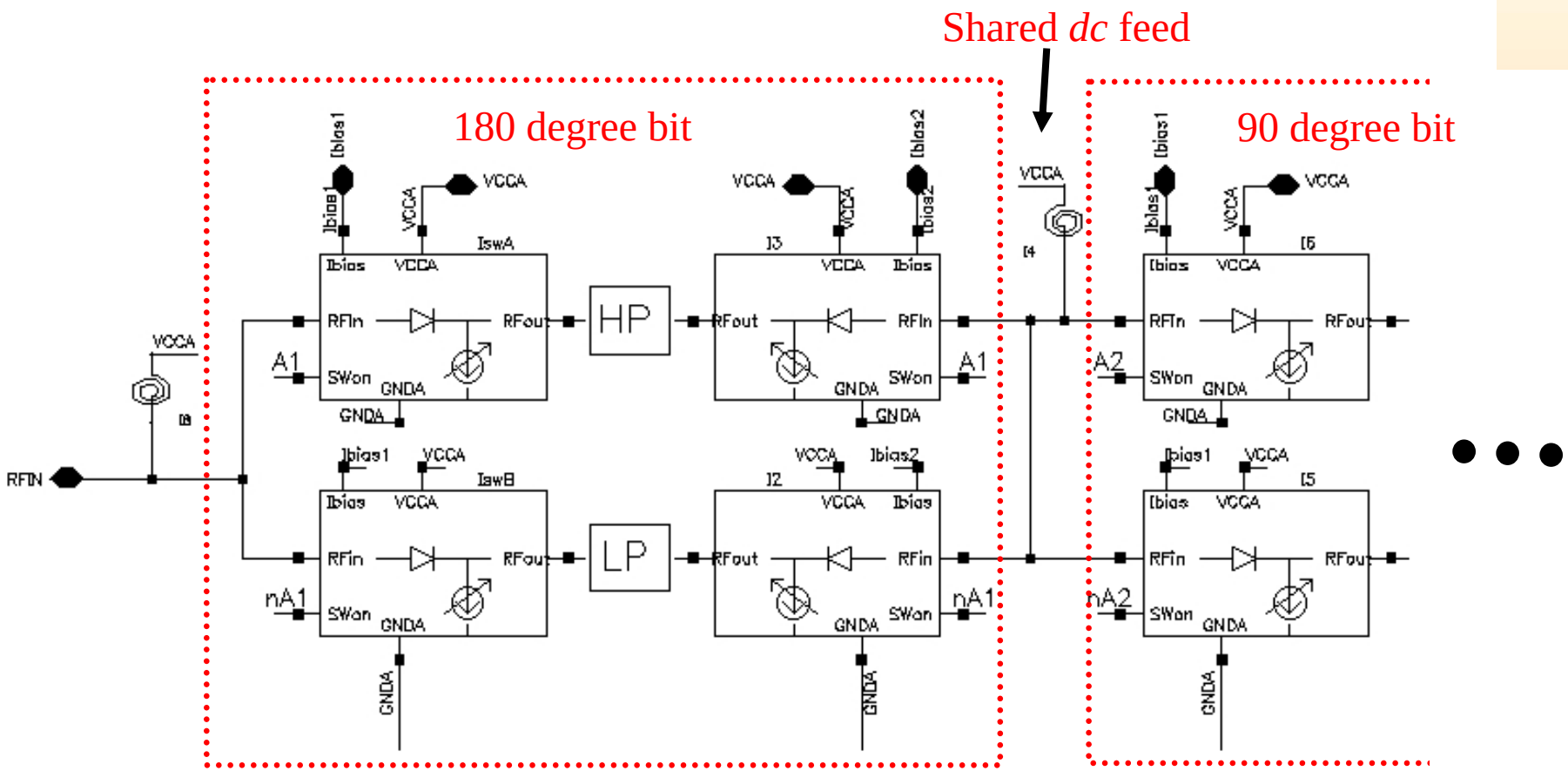


Alternative Topology



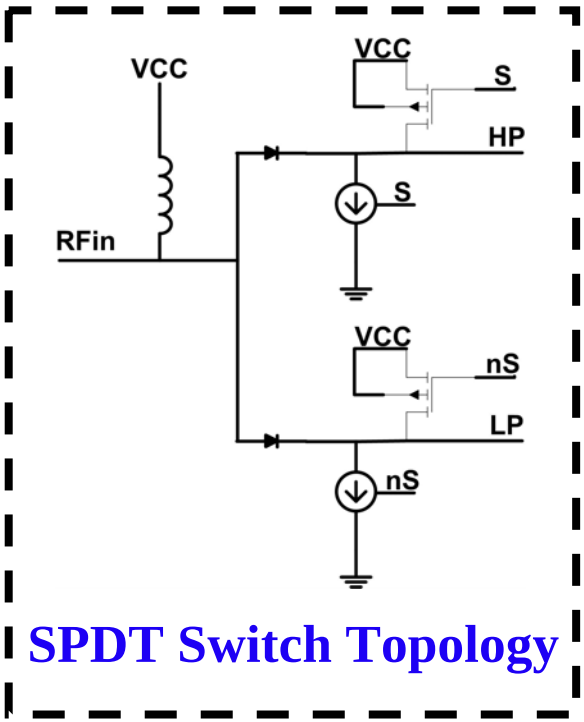
N-bit Hi-Low Pass Shifter

- **Bits may be chained together if well matched**
- **Mismatched bits cause large phase error**
- ***dc* feeds shared in between bits**

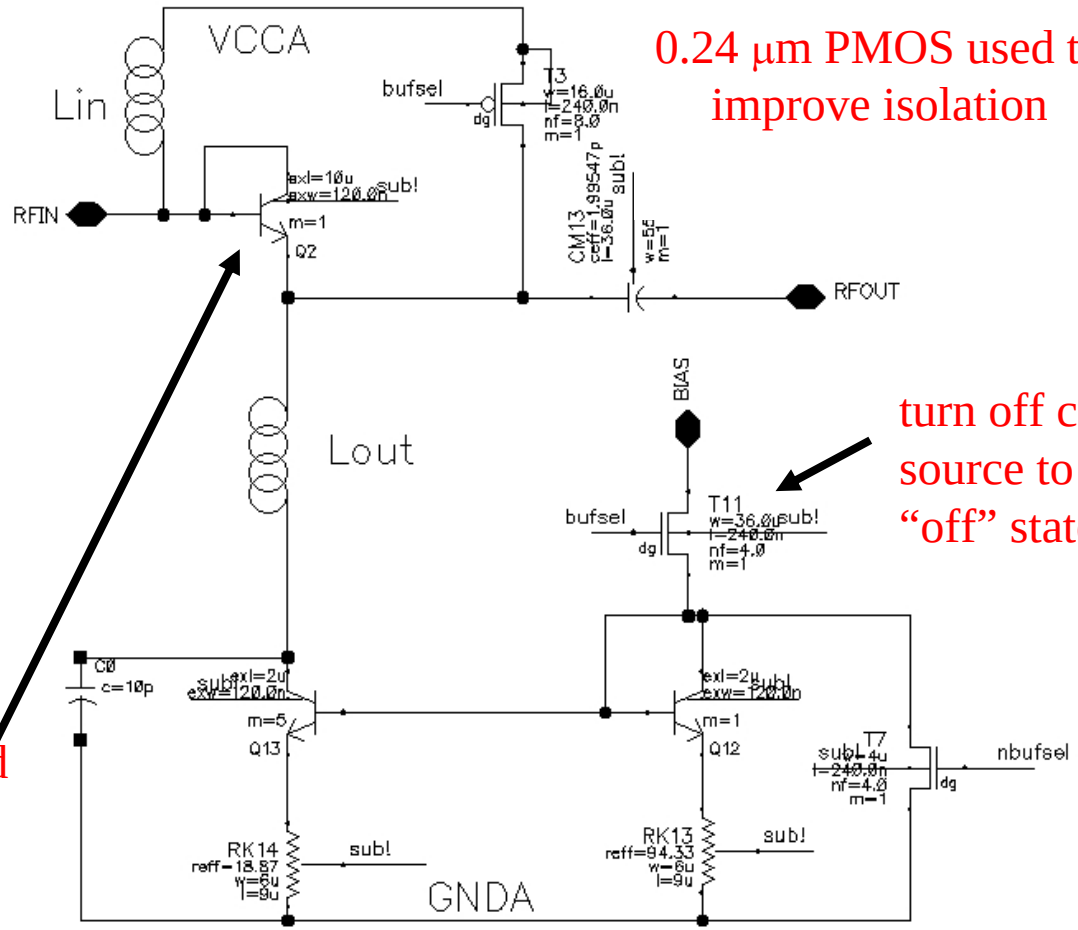


Diode Switch Design

- **Series Connected HBT Diode Element for SPDT Switch**



SPDT Switch Topology



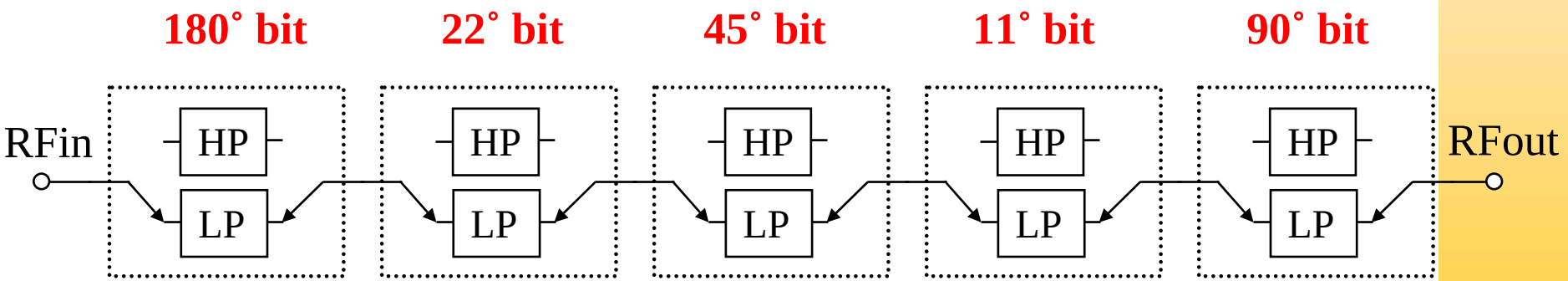
0.24 μm PMOS used to improve isolation

turn off current source to create "off" state

use of diode connected HBT npn instead of schottky or PIN diode

Bit Ordering

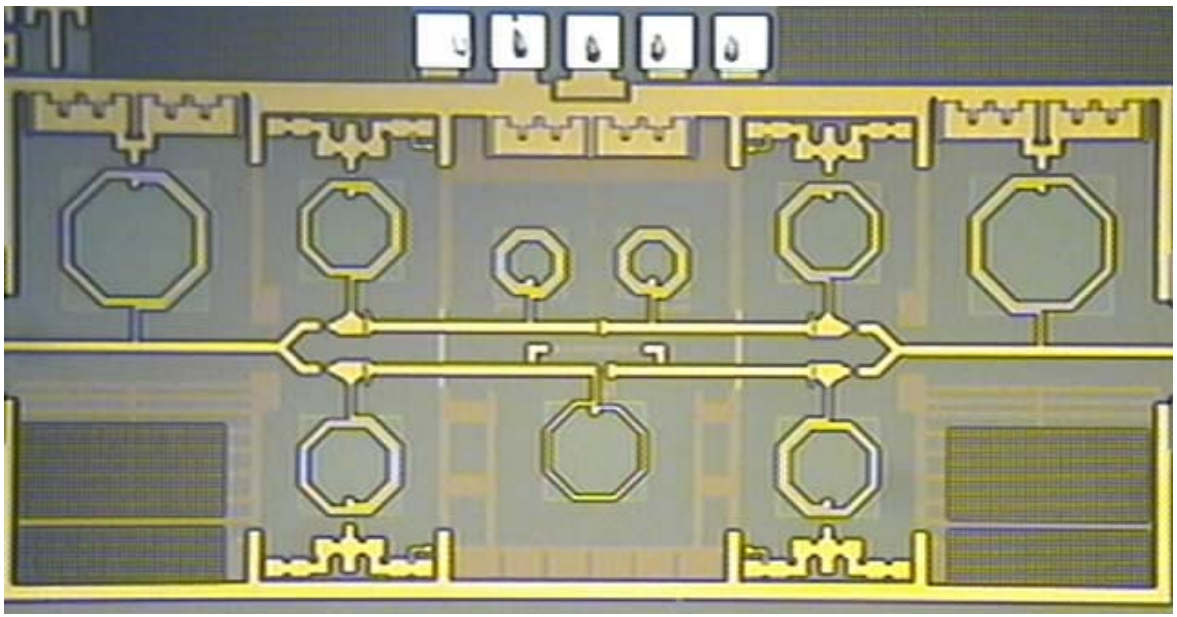
- **Higher shift value bits are easily matched (S11 < -25 dB)**
- **Smaller bits require smaller element values on low pass**
  - Parasitics cause unpredictable shift and impedance match
  - Bits can be optimized with higher values at cost of match
- **Best performance when poorly matched bits are separated**
- **Our best bit order is: 180˚ – 22˚ – 45˚ – 11˚ – 90˚**



Preliminary Results

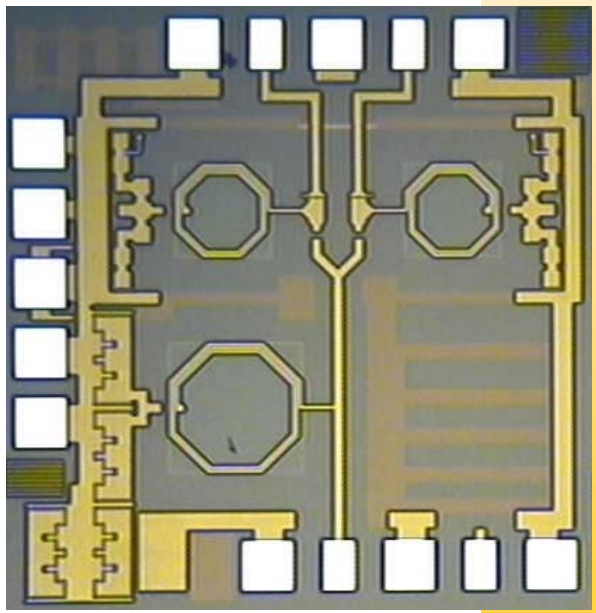
- 90° Section of Shifter and SPDT HBT Switch Fabricated
- Hardware from Jan 05 Tapeout
- Preliminary Designs

90° Section of Shifter



2.56 x 1.2 mm²

SPDT HBT Switch

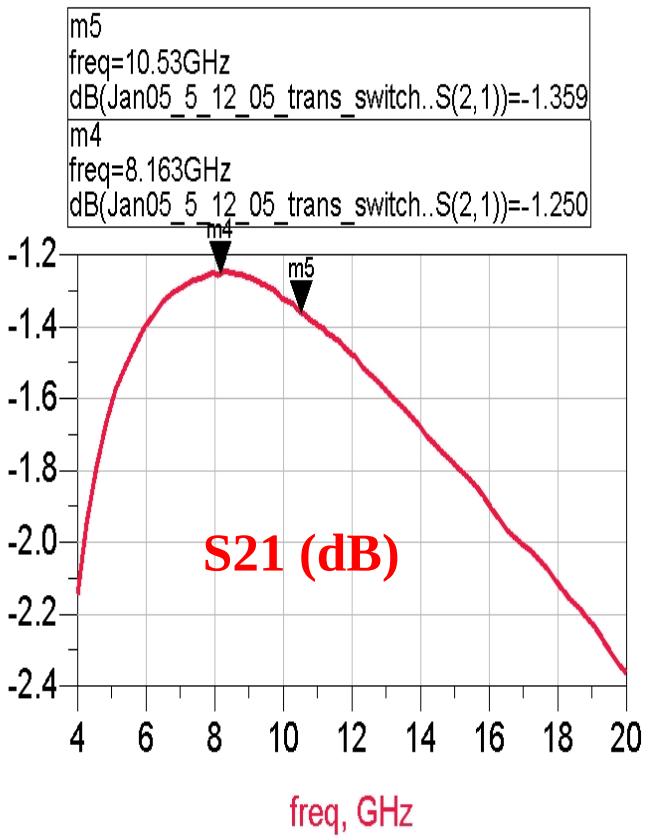


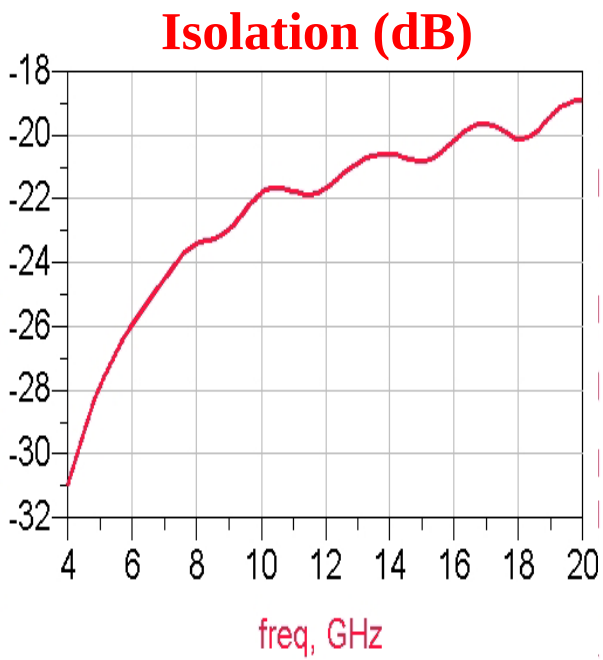
1.2 x 1.2 mm²

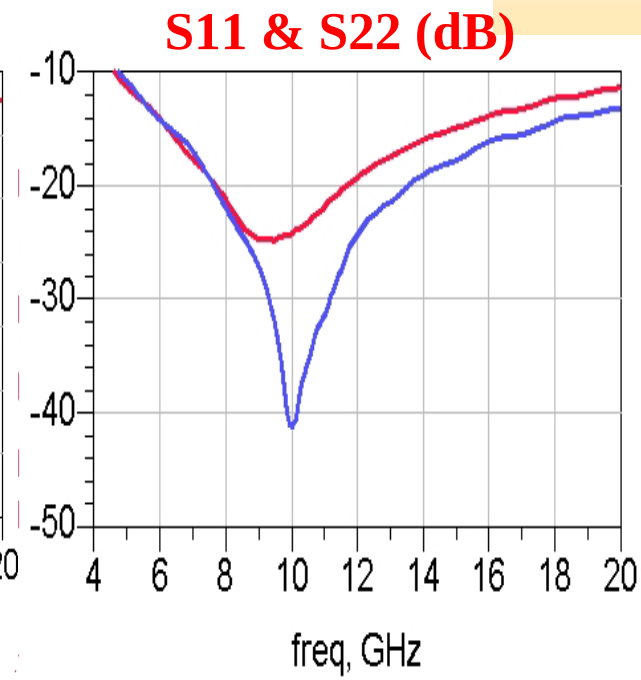
Preliminary Results

- **Single HBT Diode NPN Switch Fabricated and Tested**
- **Sim Results: IL<0.92 dB, RL>19 dB, Iso>20 dB, IIP3=24 dBm**

***dc*: Vcc=2.1V, Ibias = 1.8mA, Icc =8.75 mA**
Measured IIP3 ~ 20 dBm
Measured IP_{1dB} ~ 3 dBm



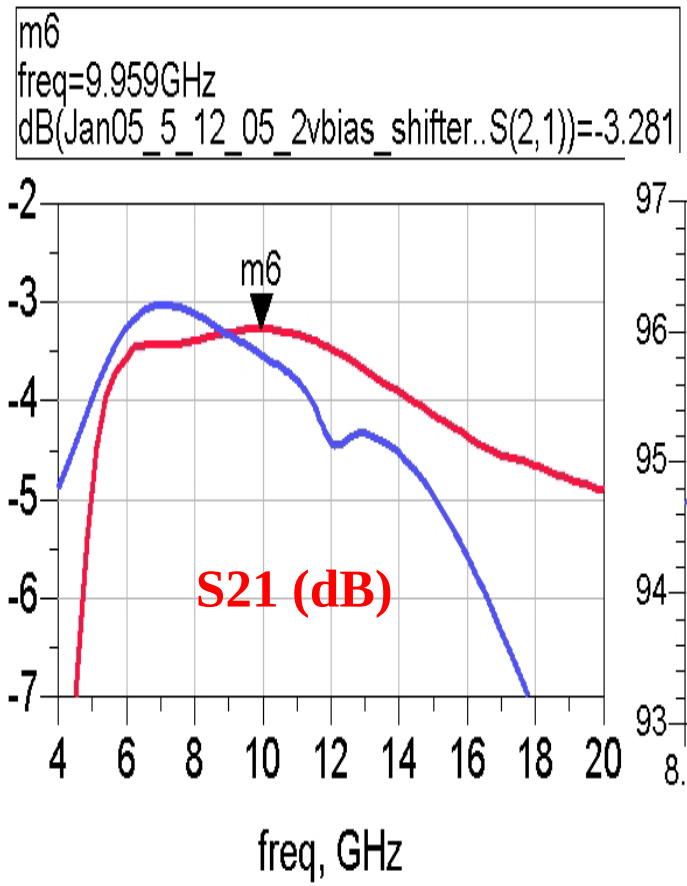




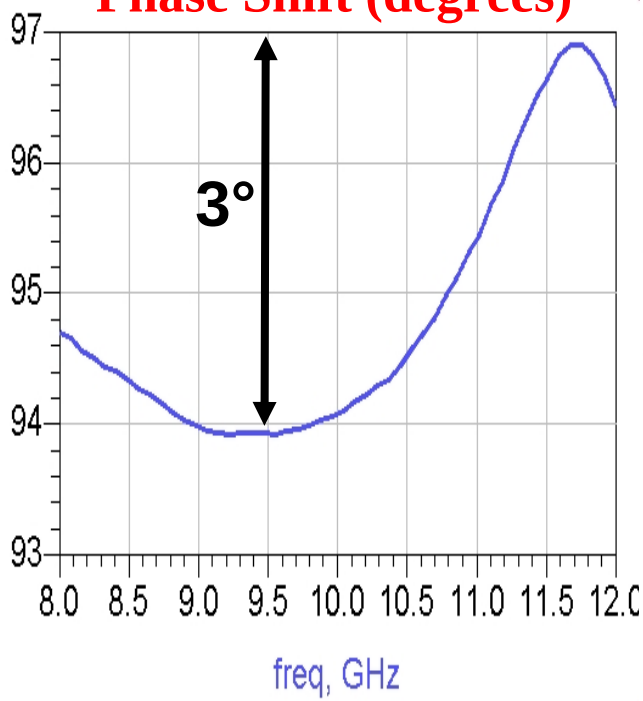
Preliminary Results

- **90° Section of Shifter Fabricated & Tested**
- **Sim. Results: IL = 2.1 dB, RL > 15, Phase Shift = 90° +/- 3°**

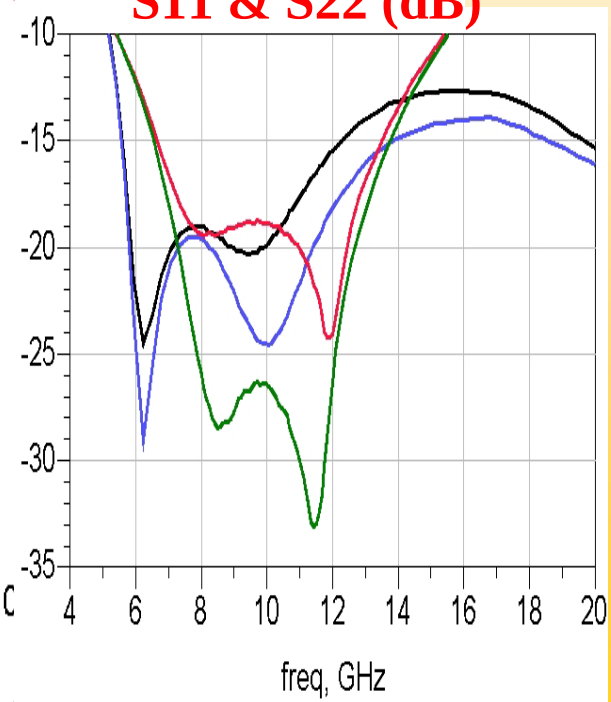
***dc*: Vcc=2.1V, Ibias1 = Ibias2 = 1.8mA, Icc =17.4 mA**



Phase Shift (degrees)

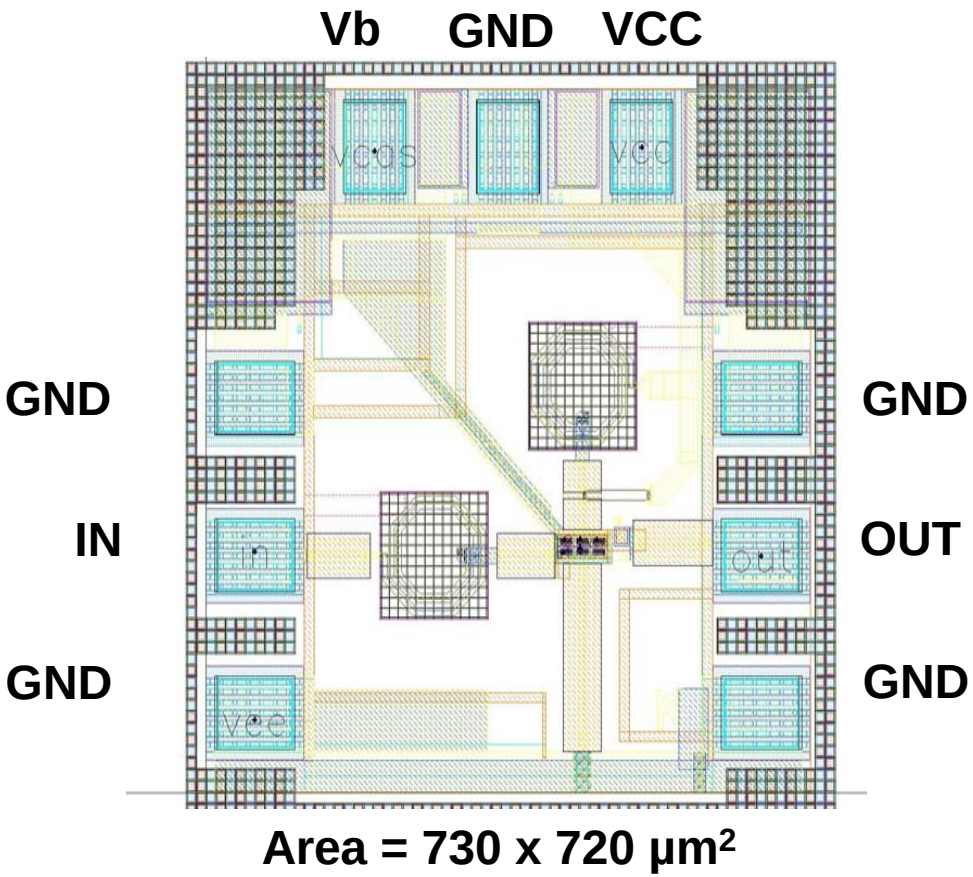


S11 & S22 (dB)



SiGe LNA

- **Layout and bias conditions**



Area = 730 x 720 μm²

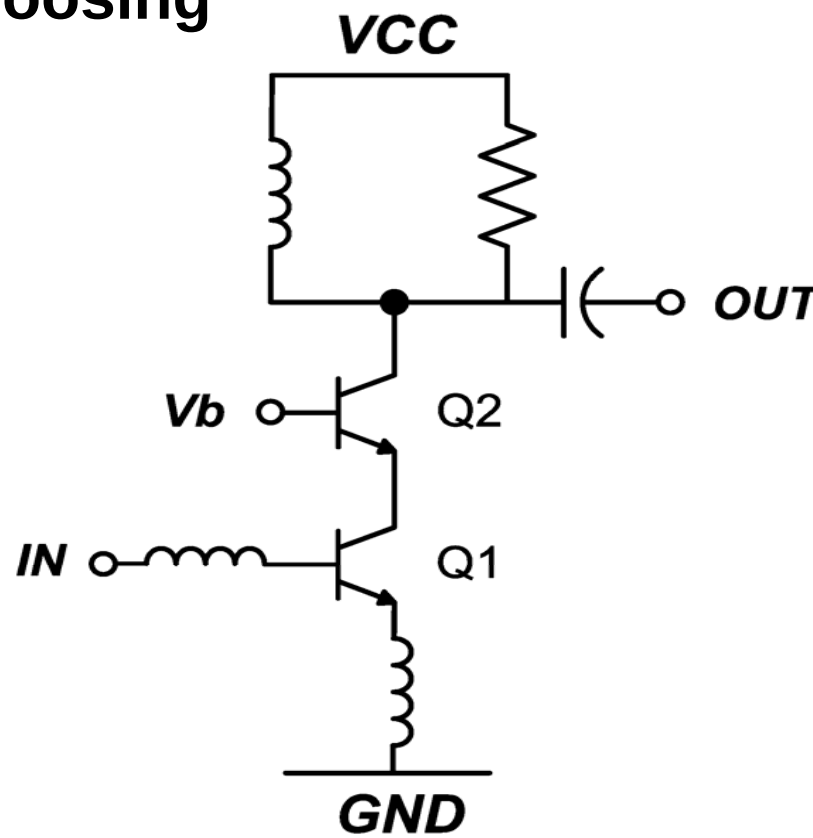
VCC	2.5 V
Vb	2 V
GND	0 V
Ib	14 uA
Ic	6 mA

SiGe LNA

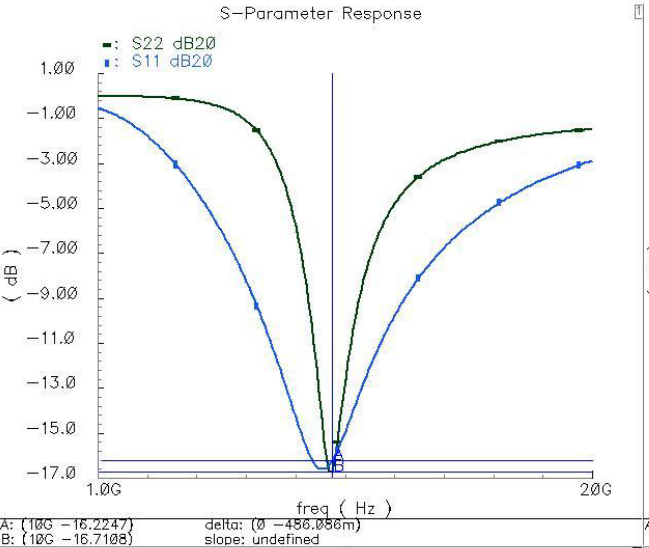
- **Cascode topology**
  - suppresses feedback and improves stability

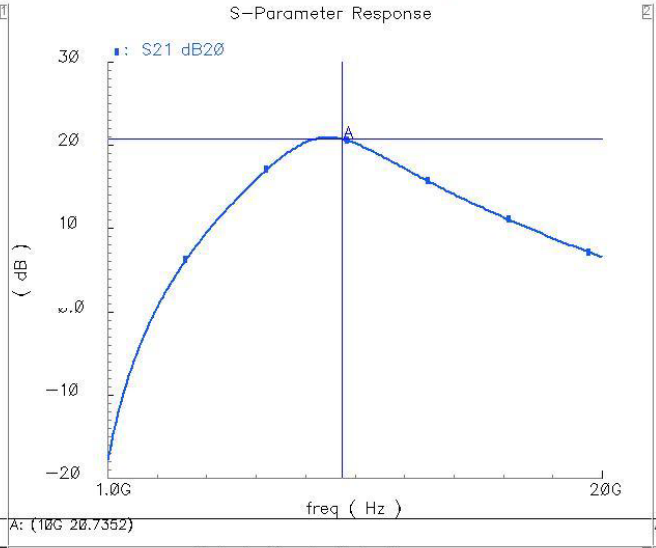
- **Noise and impedance match by choosing**
  - emitter length
  - collector current
  - base inductor
  - emitter inductor

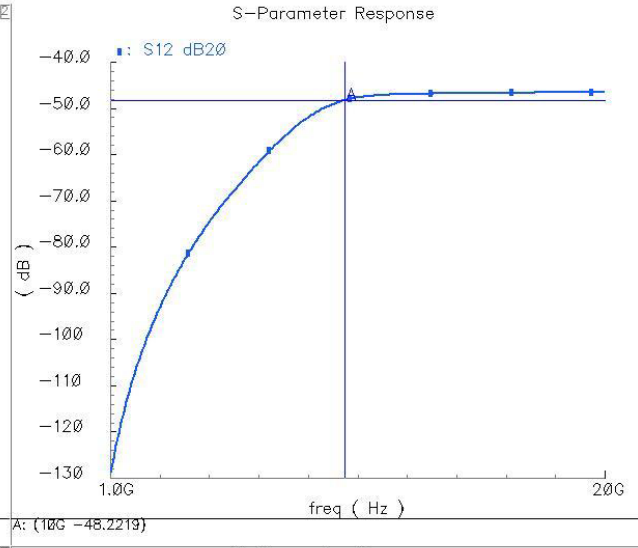
- **NF/gain/IIP3 tradeoff**

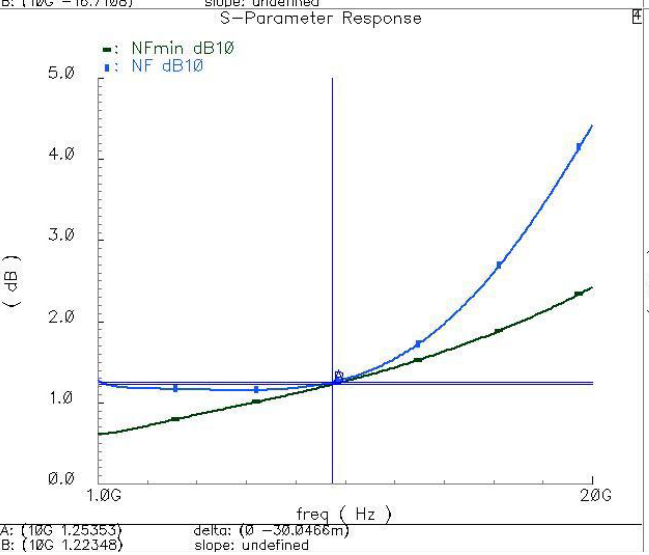


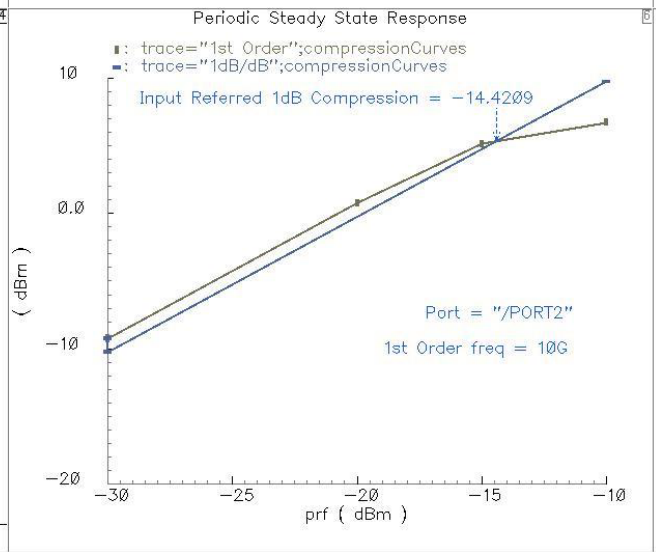
SiGe LNA

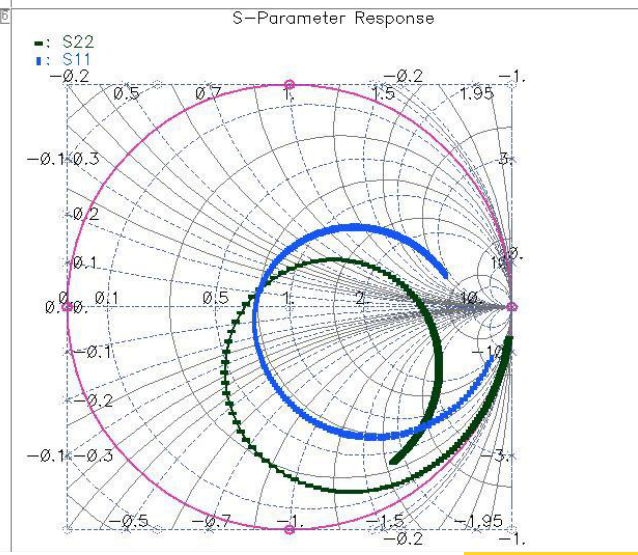

S-Parameter Response
S22 dB20
S11 dB20
1.00
-1.00
-3.00
-5.00
-7.00
-9.00
-11.0
-13.0
-15.0
-17.0
(dB)
1.0G
20G
freq (Hz)
A: (10G -16.2247)
B: (10G -16.7108)
delta: (0 -486.086m)
slope: undefined


S-Parameter Response
S21 dB20
30
20
10
-10
-20
(dB)
1.0G
20G
freq (Hz)
A: (10G 20.7352)


S-Parameter Response
S12 dB20
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100
-110
-120
-130
(dB)
1.0G
20G
freq (Hz)
A: (10G -48.2219)


S-Parameter Response
NFmin dB10
NF dB10
5.0
4.0
3.0
2.0
1.0
0.0
(dB)
1.0G
20G
freq (Hz)
A: (10G 1.25353)
B: (10G 1.22348)
delta: (0 -30.0466m)
slope: undefined


Periodic Steady State Response
trace="1st Order";compressionCurves
trace="1dB/dB";compressionCurves
Input Referred 1dB Compression = -14.420
Port = "/PORT2"
1st Order freq = 10G
10
0.0
-10
-20
(dBm)
-30
-25
-20
-15
-10
prf (dBm)

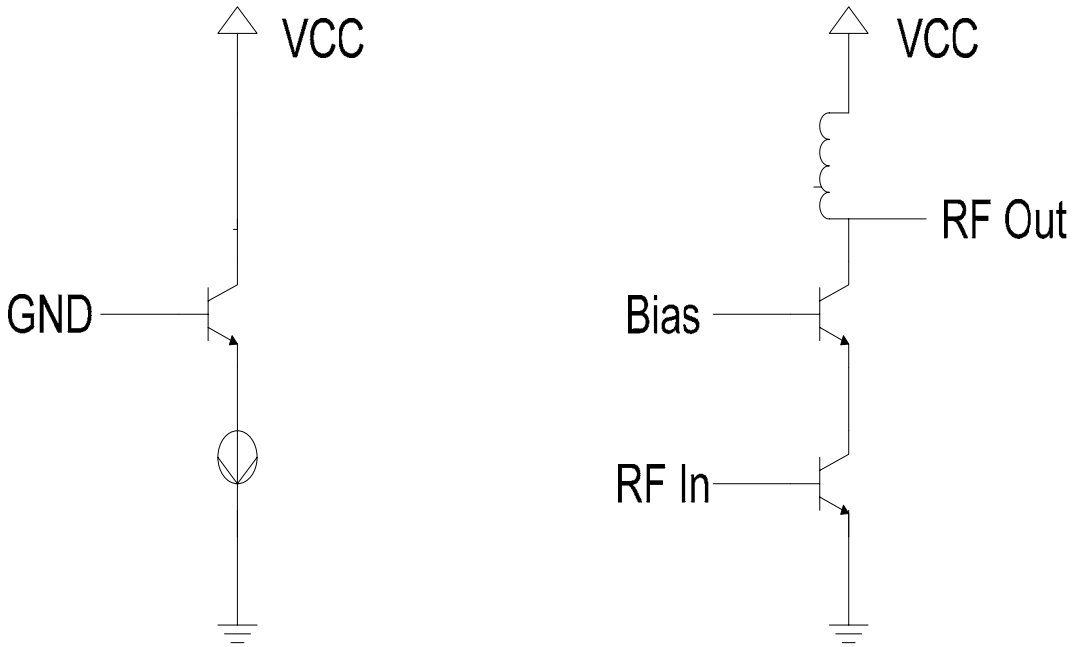

S-Parameter Response
S22
S11

SiGe LNA

- **Simulated performance summary**

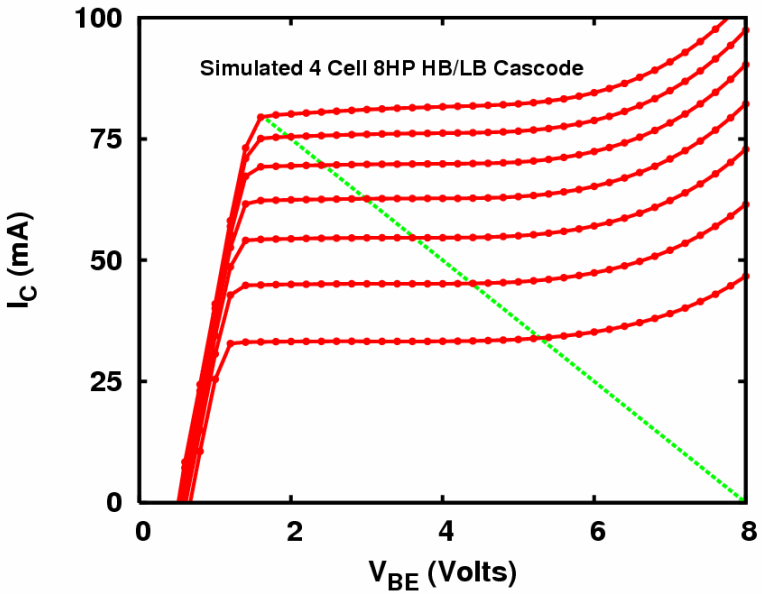
Frequency	10 GHz
S11	< -16 dB
S22	< -16 dB
S21	> 20 dB
NF	< 1.3 dB
Input P1dB	> -15 dBm

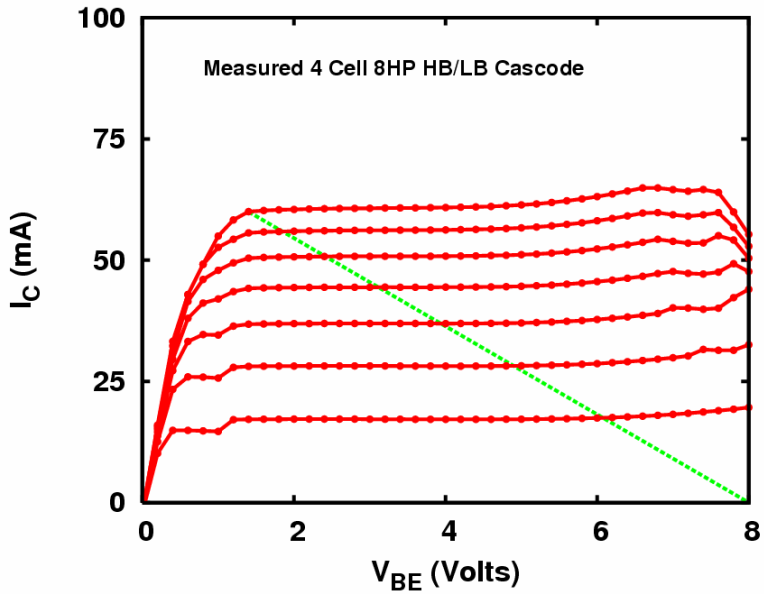
Extend PA Voltage Range



- **Forced Emitter Current**
- **Breakdown Approaches BVCBO**
- **Improves DCIV Linearity**
- **Circuit Realization of Forced I_E**
- **Upper bias is AC ground**
- **RF input on lower base**

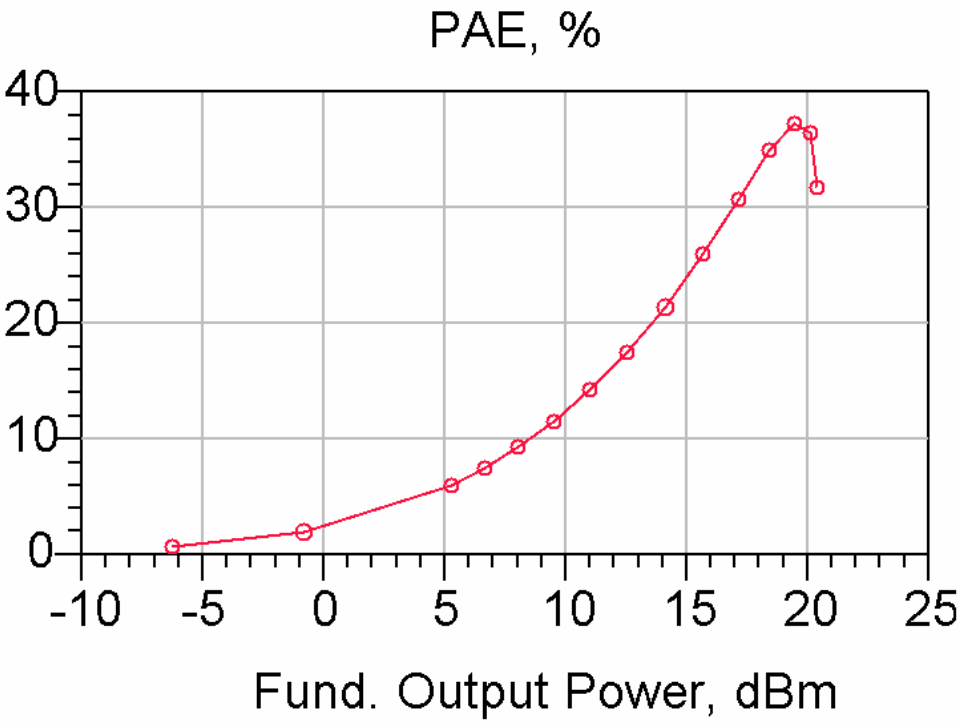
Cascode PA Characteristics





- **Simulated vs. Measured 4 Cell 8HP 0.12x18 HB / 0.12x5 LB**
- **Slight Beta difference between model and simulation**
- **Beta compression and breakdown characteristics similar**
- **Knee voltage equal to V_{BE} + V_{CESat}**

Simulated Results



8HP Cascoded Devices

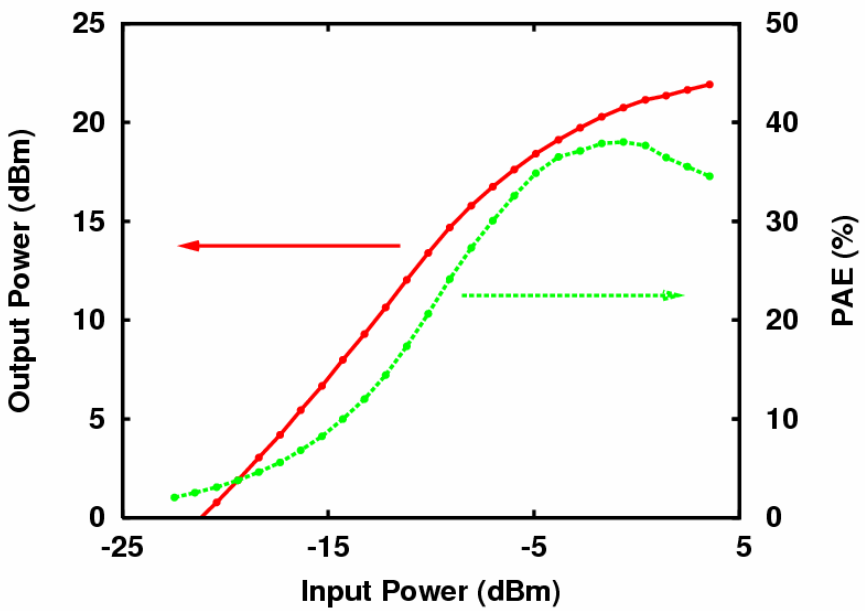
- 12 parallel load pull cells
- Post layout extraction
- Realistic on chip Qs
- Non-optimized for harmonics

Strong Class AB Results

- 19 dBm output power
- 25 dB of gain
- 38% PAE

- **Interconnects modeled using T-line models**
  - Show .1 dB of loss for 500 um run of 40 um wide line

Preliminary PA Results



- **8HP Cascoded Devices**
  - 12 parallel load pull cells
  - Non-optimized for harmonics and layout
  - Slightly mismatched source
- **Strong Class AB Results**
  - 21 dBm output power
  - 20 dB of gain
  - 38% PAE

- **Meets power spec, promising efficiency for pre-driver**
- **~150 total cascode cells to reach 30 dBm with margin for passive losses**

Summary

- MDA/AS Radar System Technology panel investing in SiGe RF devices for future radar needs
- SiGe single-chip T/R program
  - 4-year development plan (FY05-FY08)
  - First integrated T/R chips in FY07
  - Requirements developed (FY05)
  - Critical devices designed and analyzed (FY05)
  - Some devices fabricated and tested (FY05)
  - More fabrication runs underway (due back late FY05)
  - Critical risk reduction for low power density apertures
- *SiGe Single-chip T/R for Radar appears feasible*